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From Source Control to Path Collaboration: A Review of Development Trends in Thermal Management Technologies for High-Power Electronic Devices

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Abstract

The heat flux density of high-power electronic devices continues to rise, and the thermal dissipation bottleneck has become a key factor limiting the performance of wide and ultra-wide bandgap semiconductors.From a full-chain thermal management perspective of "from source to path," this paper systematically reviews the evolution trajectory of source-level thermal resistance control during chip manufacturing and thermal path collaborative management after chip operation.The review indicates that thermal management concepts are undergoing a triple paradigm shift: from post-hoc cooling to source-level control, from single-method optimization to full-chain collaboration, and from fixed-mode operation to intelligent adaptive cooling.Recent breakthroughs have been achieved in areas such as thermal interface resistance control of β-Ga_2O_3/diamond heterojunctions, although shortcomings remain in high-performance thermal interface materials and wafer bonding equipment.This paper can serve as a reference for the selection of thermal management solutions for high-power-density packaging and the planning of technology roadmaps.

Keywords

High-power Electronic Devices; Thermal Management; Wide Bandgap Semiconductors; Gallium Oxide; Cooling Technologies.

1. Introduction

With the rapid development of new energy grid integration, electric vehicles, rail transit, data centers and other fields, wide and ultra-wide bandgap power devices represented by silicon carbide (SiC), gallium nitride (GaN), and gallium oxide (β-Ga_2O_3) are accelerating their iteration, leading to a continuous rise in the heat flux density of power devices, with local heat flux potentially exceeding 10 kW/cm^2 [1].Traditional post-hoc cooling methods are gradually approaching their performance limits, and thermal management has evolved from an auxiliary reliability factor to a core constraint determining the power ceiling, service life, and system stability of devices [2].Temperature rise significantly exacerbates the thermomechanical failure risk of power devices, easily leading to issues such as bond wire lift-off and chip cracking, which severely restrict device performance and system reliability [3].To date, researchers in China have conducted extensive studies on mainstream cooling methods such as air cooling, liquid cooling, and heat pipes [3-4].However, existing reviews mostly focus on a single cooling method or specific device cooling solutions, and rarely synthesize the full-chain temporal perspective of "chip manufacturing – heat transfer – intelligent control", thus lacking sufficient elaboration on the intrinsic evolution logic of "source-level thermal resistance reduction" and "thermal path collaboration".With the rapid development of ultra-wide bandgap semiconductors, devices face inherent bottlenecks such as low intrinsic thermal conductivity

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and high heterogeneous interface thermal resistance [5], making traditional "post-hoc cooling" design concepts unable to meet the high heat dissipation requirements of next-generation power devices.In this context, this paper takes "from source to path" as the main line, dividing thermal management technologies for high-power devices into three progressive stages: source-level thermal resistance control during chip manufacturing and thermal path collaborative management during operation. It systematically reviews the research progress of key technologies such as epitaxial optimization, interface engineering, near-junction cooling, heat extraction–spreading–rejection collaboration, composite integration, and intelligent thermal management. It summarizes the paradigm shift patterns in the thermal management field from passive heat dissipation to proactive source-level control, from single-method optimization to full-chain collaboration, and from fixed-mode cooling to intelligent adaptive cooling. It also looks forward to future development trends and breakthrough directions, aiming to provide a reference for thermal management design and technology roadmap planning for high-power-density devices.

2. Thermal Dissipation Challenges and Technology Evolution Path for High-Power Devices

2.1. Increasing Heat Flux Density and Escalating Thermal Dissipation Bottlenecks

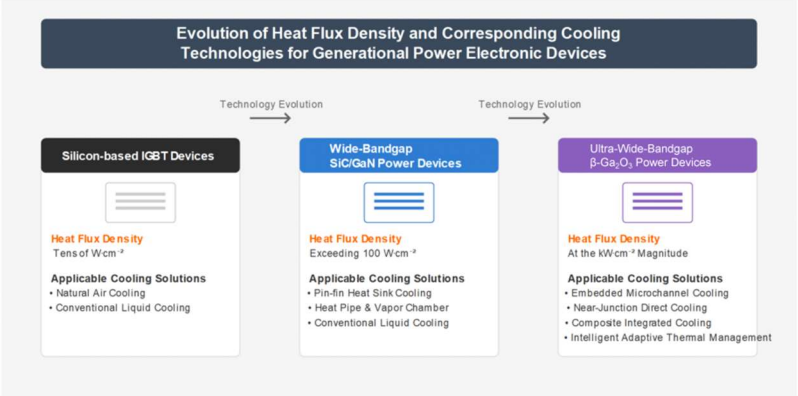

Figure 1. Evolution of heat flux density in power devices and corresponding cooling technologies.

From silicon-based IGBTs to SiC/GaN wide bandgap devices and then to β-Ga_2O_3 ultra-wide bandgap devices, power density continues to increase power density has undergone stepwise escalation, and thermal management difficulty rises exponentially.Traditional silicon-based devices have a heat flux density of about tens of W/cm^2, where air cooling and conventional liquid cooling can meet the requirements.High-power power electronic chips can reach a heat flux density of over 100 W/cm^2 [5], and efficient cooling methods such as liquid-cooled pin fins are increasingly widely used.Ultra-wide bandgap β-Ga_2O_3 devices have a breakdown field strength and Baliga's figure of merit far exceeding those of traditional semiconductor materials [5];However, the intrinsic thermal conductivity of β-Ga_2O_3 is only 10–27 W/(m·K), and the

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thermal conductivity exhibits strong anisotropy. The traditional end-of-pipe concept of "additional cooling after packaging" is no longer sufficient, and must extend to source-level control during chip manufacturing.Figure 1 illustrates the generational evolution characteristics of heat flux density ranges and mainstream cooling technologies for typical power devices from traditional silicon-based to future extreme scenarios. This intuitively demonstrates the urgent need for a "generational leap" in thermal management.

2.2. Three-Stage Evolution of Thermal Dissipation Technologies

Based on the timing of thermal management intervention, this paper constructs a three-stage technology evolution framework of "source control–path collaboration – intelligent adaptive grading" as shown in Figure 2.Among them, the first stage focuses on heterogeneous interface thermal resistance and low-resistance interconnects during chip manufacturing.The second stage covers the full-chain collaboration of heat extraction, heat spreading, and heat rejection.The third stage introduces dynamic current limiting and three-dimensional thermal field sensing, achieving a leap from passive heat dissipation to active temperature control.Detailed design strategies and verification of Stage 3 intelligent thermal regulation will be elaborated in Section 5.

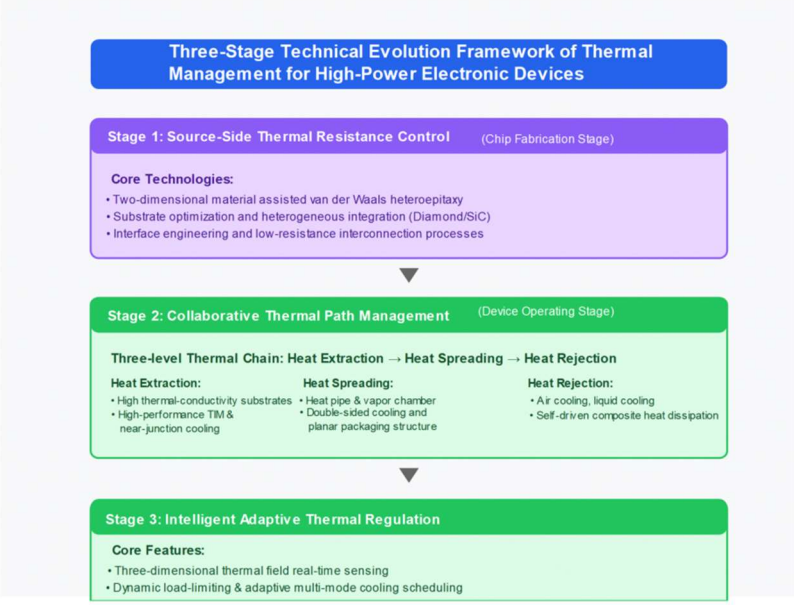

Figure 2. Evolution framework of thermal management technologies for high-power devices: from source control to intelligent adaptive cooling.

Stage 1: Source-level thermal resistance control (chip manufacturing stage). Centered on heterogeneous interface thermal resistance regulation, through means such as epitaxial structures, buffer layers, two-dimensional material insertion, and heterogeneous substrate integration, thermal resistance is reduced during chip growth and packaging manufacturing, achieving inherent thermal resilience at the source.

Stage 2: Thermal path collaborative management (chip operation stage). Aiming for efficient heat transport, following the three-level path of "heat extraction – heat spreading – heat rejection," it collaborates the substrate, thermal interface material, vapor chamber, heat sink and other links to achieve full-chain efficient heat dissipation.

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3. Source-Level Thermal Resistance Control: Low-Thermal-Resistance Design Technologies During Chip Manufacturing

3.1. Core Bottleneck of Heterogeneous Interface Thermal Resistance

Wide and ultra-wide bandgap devices often adopt heterogeneous epitaxial structures, such as GaN-on-Si and β-Ga_2O_3-on-diamond. Lattice mismatch and coefficient of thermal expansion mismatch cause strong interfacial phonon scattering, resulting in significant interface thermal resistance, which is the core bottleneck restricting device heat dissipation performance.Traditional direct bonding and epitaxial technologies easily produce amorphous layers, defects, and high stress, making it difficult to balance crystal quality and heat dissipation performance.

3.2. Interfacial Thermal Resistance Reduction for β-Ga_2O_3/Diamond Heterojunctions

The integration of β-Ga_2O_3 with diamond is hindered by large lattice mismatch and CTE mismatch, leading to high interfacial thermal resistance (ITR). As summarized in a recent review [6], several research groups have explored surface-activated bonding (SAB) to achieve low-temperature or room-temperature GaN-on-diamond bonding. For instance, BAE Systems demonstrated GaN-on-diamond bonding below 150 °C, Mu et al. achieved room-temperature bonding with a 27 nm Si interlayer, and Fujitsu reported an ITR of 67 m^2·K/GW [6].

A significant breakthrough was reported by Ning et al. [7], who introduced a monolayer graphene as a van der Waals interface buffer layer on polycrystalline diamond, enabling controllable epitaxy of β-Ga_2O_3 thin films. This structure reduces the β-Ga_2O_3/diamond ITR to 2.82 m^2·K/GW [7], approximately one order of magnitude lower than the values reported for conventional SAB methods (e.g., 67 m^2·K/GW [6]). This opens a new path for near-junction heat dissipation, though wafer-scale production remains a challenge.

3.3. Substrate Optimization and Heterogeneous Integration Technology

High-thermal-conductivity substrates are fundamental to reducing source-level thermal resistance. Harbin Institute of Technology, in collaboration with the Russian Academy of Sciences, has achieved a single-crystal diamond with a thermal conductivity of 2400 W/(m·K) [6]. A diamond/copper composite heat sink for GaN power amplifiers has demonstrated a practical thermal conductivity of 564.2 W/(m·K) in microchannel applications [8]. For practical applications, diamond/copper composites offer a balance between thermal conductivity (500–600 W/(m·K)) and CTE matching (4–6 ppm/K) [9]. High-quality single-crystal diamond with a thermal conductivity of 2229.3 W/(m·K) has also been reported [10].

Heterogeneous integration can be realized through: (1) wafer bonding (e.g., surface-activated bonding) enabling low-temperature bonding [6]; (2) ion-cutting for β-Ga_2O_3-on-SiC or β-Ga_2O_3-on-diamond structures; and (3) substrate thinning to shorten the heat conduction length (typically 50–100 μm). The thermal extraction performance during device operation is discussed in Section 4.1.

3.4. Interface Engineering and Low-Resistance Interconnect Processes

Interconnect processes such as nano-silver sintering and transient liquid phase bonding (TLP) can reduce interface thermal resistance and improve device high-temperature resistance and long-term reliability [11].Planar interconnects, copper clip packaging, and double-sided cooling structures can reduce parasitic inductance and thermal resistance, improve device overcurrent capability and heat dissipation uniformity, and meet the requirements of high-reliability, high-power-density packaging [11].

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4. Thermal Path Collaborative Management: Full-Chain Heat Dissipation Technologies After Chip Operation

4.1. Heat Extraction: Near-Junction Rapid Heat Removal

Heat extraction removes heat from the chip junction region using substrates and TIMs engineered during manufacturing (Section 3.3). The performance is quantified by measurable parameters.

Diamond-based substrates have demonstrated strong heat extraction. A diamond/copper composite heat sink achieved a total thermal resistance of 0.064 K/W under single-phase immersion cooling, with the Nusselt number increasing by 14.4% [8]. In GaN power amplifiers, replacing a Cu/Mo/Cu heat sink with a diamond/Cu composite reduced the channel temperature by 12 °C under 400 W/cm^2 [9]. Embedded microchannels have sustained heat fluxes exceeding 1,000 W/cm^2 with surface temperatures below 100 °C [8][10].

Diamond-based microchannel heat sinks (MCHS) offer higher capability. As reported by Qi et al. and summarized by Lan et al. [1], a diamond MCHS achieved a heat transfer coefficient of 5,637–11,447 $W/(m^2 \cdot K)$ under 40–120 W/cm^2, representing a 37%–73% improvement over aluminum MCHS [1].

Thermal interface materials also play a role. Surface-activated bonding (SAB) has reduced interfacial thermal resistance to values as low as 67 $m^2 \cdot K/GW$ [1][6].

4.2. Heat Spreading: Hot Spot Temperature Uniformization

Heat spreading flattens concentrated hot spots and reduces local thermal stress.Heat pipes and vapor chambers (VCs) rely on phase-change cycles to achieve ultra-high equivalent thermal conductivity, which can improve device temperature uniformity.Compared with double-sided heat pipe radiators, the 3D composite phase change radiator reduces thermal resistance by 7.8%–10.5% under the same wind speed and power conditions [12].Double-sided cooling packaging enables heat dissipation from both sides of the chip, resulting in a more uniform junction temperature distribution [11].

4.3. Heat Rejection: Efficient Dissipation to the Environment

4.3.1. Air Cooling:

low cost, simple structure, suitable for medium and low power density scenarios; heat dissipation capability can be improved through fin optimization and flow channel design.

4.3.2. Liquid Cooling:

mainly includes typical forms such as cold plates, microchannels, jet impingement, and immersion cooling. The use of pin-fin structures and manifold microchannel designs can significantly enhance convective heat transfer [3].

4.3.3. Self-driven And Synergistic Heat Dissipation:

a liquid metal self-driven heat dissipation system utilizes waste heat to drive the circulation, improving heat dissipation efficiency by 116% compared to natural cooling [13];Thermoelectric cooling coupled synergistically with liquid cooling can achieve both dynamic fast response and efficient heat rejection characteristics.

As shown in Figure 3, this paper summarizes the key performance indicators and enhancement effects of representative solutions in the full-chain heat dissipation path according to the three-level link of heat extraction, heat spreading, and heat rejection.

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Figure 3. Classification and performance enhancement summary of full-chain thermal path management technologies.

5. Paradigm Shift: From Composite Integration to Intelligent Adaptive Cooling

5.1. From Single Means to Composite Integration

Current thermal management technologies have entered a multi-mode collaborative stage, which mainly includes:

5.1.1. Multi-technology Collaboration:

phase-change buffering, heat pipe spreading, and liquid cooling rejection in series, balancing thermal buffering, temperature uniformization, and efficient heat rejection.

5.1.2. Material-structure Integration:

diamond microchannel substrates and GaN-on-diamond near-junction integration achieve coupling of high thermal conductivity and efficient convection.

5.1.3. Packaging-cooling Collaboration:

the combination of double-sided cooling and planar interconnect structures can simultaneously reduce module thermal resistance and parasitic inductance [11].

5.2. From Fixed Operation to Intelligent Adaptive Cooling

Intelligent thermal management has become the core trend of next-generation thermal management, achieving "on-demand cooling and precise temperature control":

5.2.1. Three-dimensional Thermal Field Sensing:

multi-sensors monitor junction temperature, heat flux, and hot spot distribution in real time, capturing temperature anomalies at the millisecond level.

5.2.2. Active Thermal Control and Dynamic Current Limiting:

adjusting current, switching frequency, and power loss based on junction temperature feedback, utilizing device thermal inertia to enhance short-term overload capability.

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5.2.3. Adaptive Multilevel Scheduling:

automatically switching among air cooling, liquid cooling, phase-change buffering and other modes according to thermal load, improving energy efficiency and reliability.

Thermal management technologies are undergoing a triple paradigm shift: post-hoc cooling → source-level control; single-method optimization → full-chain collaboration; fixed operation → intelligent adaptation.

6. Critical Assessment and Future Directions

6.1. Global Research Landscape

Internationally, led by DARPA programs such as NJTT and ICECool, a complete innovation chain from materials and structures to systems has been established in areas such as near-junction heat transport and embedded microchannels.In China, notable breakthroughs have been achieved in source-level and integration directions such as van der Waals epitaxy of β-Ga_2O_3 on diamond, diamond heat spreaders, and composite phase-change cooling – for example, a thermal boundary resistance as low as 2.82 m^2·K/GW was reported [7].However, high-performance thermal interface materials, high-precision wafer bonding equipment, and manufacturing tools for embedded microchannels remain in the early stages of development and require sustained research efforts.

6.2. Remaining Challenges

The dynamic matching mechanisms of multi-technology collaborative cooling lack systematic experimental validation and quantitative models.

Intelligent adaptive cooling largely remains at the conceptual stage, with insufficient practical scheduling algorithms and validation platforms.

The electro-thermo-mechanical coupling failure mechanisms of ultra-wide bandgap devices still require further in-depth elucidation.

6.3. Future Directions

6.3.1. Source-level Thermal Management Intensification:

Van der Waals-assisted heteroepitaxy, heterogeneous integration with single-crystal diamond, and near-junction direct cooling are expected to become mainstream directions.

6.3.2. System-level Thermal Path Integration:

Collaborative design integrating substrate, TIM, vapor chamber, and heat sink to minimize overall thermal resistance.

6.3.3. Smart Thermal Management:

On-chip thermal sensors, intelligent driver chips, and adaptive multilevel cooling are expected to achieve large-scale application.

6.3.4. Indigenous Development of Key Materials and Equipment:

Achieving breakthroughs in high-thermal-conductivity materials, low-thermal-resistance interconnection processes, and advanced packaging equipment to establish a complete technology industry chain.

7. Conclusion

In summary, the thermal management technologies for high-power devices have formed a clear development trajectory of "source-level interface regulation–three-stage path collaboration–intelligent adaptive cooling."In the next five years, van der Waals-assisted heteroepitaxy is expected to expand from β-$Ga_2O_3$to broader material systems such as GaN-on-

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diamond.Heterogeneous integration of on-chip micro thermal sensors and driver ICs will promote the birth of smart thermal management chips with "self-sensing, self-decision, and self-cooling" capabilities.In the direction of source-level thermal resistance reduction, Chinese researchers have made significant progress (e.g.,).Future research should focus on the development of heterogeneous integration equipment and high-performance thermal interface materials to further enhance device reliability and performance.

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