ISSN: 2664-9640

A Review of Low-Power Circuit Design for the Internet of Things based on CMOS

Jingchao Sun*

School of Physics, Changchun University of Science and Technology, Changchun, Jilin, 130022, China

*Corresponding author's e-mail: 1321310200@qq.com

Abstract

With the deployment of IoT nodes reaching the hundreds of billions, power consumption has become a key bottleneck limiting the operational lifespan and size of battery-powered and environmental energy harvesting nodes. Consequently, the design of ultra-low-power circuits operating at the nW–pW level using CMOS processes has emerged as a central issue in this field.This paper, themed 'CMOS-based Low-Power Circuit Design for the Internet of Things', systematically reviews and analyses 45 representative publications from 2012 to 2026, providing a comprehensive overview across various module dimensions including voltage and current reference sources, RF front-ends, power amplifiers, transceiver systems, digital and security circuits, and power management and energy harvesting.Analysis indicates that through technological innovations such as all-CMOS sub-threshold references, inductorless RF topologies, adiabatic logic, and adaptive duty-cycle power management, the power consumption of each module has steadily decreased from the early milliwatt range to the nW and even pW levels; advanced process nodes have extended from 0.18 μm to 7 nm FinFET, further enhancing energy efficiency and integration.However, existing research has largely focused on the performance limits of individual modules, lacking collaborative design verification that integrates the reference, front-end, power management and digital control into a complete system; furthermore, robustness data under process variations, electromagnetic interference and long-term ageing conditions remains relatively scarce.This review highlights that future research must seek an optimal trade-off between power consumption, performance and reliability in single-chip system integration, providing a reference for the fully integrated ultra-low-power design of passive and semi-passive IoT nodes.

Keywords

Internet of Things; Low Power; CMOS.

1. Introduction

With the rapid proliferation of the Internet of Things, the number of IoT nodes has reached the tens of billions and has been widely deployed in fields such as environmental monitoring, smart wearables, logistics management and industrial sensing. Most of these nodes rely on batteries or environmental energy harvesting for power, and their operational lifespan and size are strictly constrained by the overall power consumption of the chip. Therefore, reducing circuit power consumption to the microwatt or even nanowatt level whilst maintaining the required performance has become a core challenge in IoT chip design.Complementary Metal-Oxide-Semiconductor (CMOS) technology, with its high integration, low static power consumption and continuously shrinking feature sizes, has become the primary platform for realising low-power IoT circuits. Centring on the theme of 'CMOS-based low-power IoT circuit design',

ISSN: 2664-9640

researchers have conducted in-depth explorations across multiple dimensions, including reference sources, RF front-ends, power amplifiers, transceivers, power management, and digital and security circuits.This paper has collected 45 representative publications released between 2012 and 2026 through searches of domestic and international journals, theses, and scientific and technological achievement databases, covering multiple process nodes ranging from 180 nm to 7 nm FinFET. These publications systematically illustrate the evolution of low-power design from milliwatts to picowatts, and their research approaches and circuit architectures provide a fundamental reference for the conduct of this study.The following sections will organise and review the aforementioned literature according to functional modules.

Literature Search Strategy

To ensure comprehensive coverage of recent advances in CMOS-based low-power circuit design for IoT applications, literature retrieval was conducted using major domestic and international databases, including IEEE Xplore, ScienceDirect, Web of Science, Google Scholar, CNKI, and university thesis repositories. The search period covered publications from 2012 to 2026, using keywords such as “CMOS low-power circuit”, “Internet of Things”, “ultra-low power”, “RF front-end”, “power management”, “energy harvesting”, and related combinations. Inclusion criteria comprised studies reporting circuit architectures, design methodologies, measured or simulated low-power performance, and implementations targeting IoT applications. Studies with insufficient technical details, duplicated reports, non-CMOS implementations, or research unrelated to low-power IoT systems were excluded. Following screening and classification, 45 representative publications were selected for further review and analysis.

2. CMOS Low-Power Circuit Design Techniques

2.1. Voltage and Current Reference Sources

In the realm of ultra-low-power voltage and current reference circuits, the reference source serves as the foundation of all analogue and mixed-signal systems; its own power consumption directly determines the energy baseline in the open-loop domain. To overcome the constraints imposed by bipolar junction transistors (BJTs) in traditional bandgap references regarding supply voltage and power consumption, researchers have generally shifted towards all-CMOS subthreshold design schemes.Pallavi et al. (2026) [1] proposed a low-power, high-stability CMOS bandgap reference for wearable IoT devices. This circuit integrates a zero-temperature-coefficient current generator with a temperature-compensated resistor network, and introduces a two-stage self-timed start-up mechanism and a subsequent adjustment stage, effectively resolving the trade-off between accuracy, power consumption and circuit complexity.Yang Jingci (2023) [2] designed three all-CMOS voltage reference circuits specifically to address the challenges of significant energy fluctuations and low available voltages in passive IoT nodes.The first multi-output nano-watt circuit utilises a multi-loop active load to achieve a line regulation of 0.05%/V at a power consumption of 64.7 nW; the second op-amp-free sub-nano-watt circuit further reduces power consumption to 0.752 nW through a self-biased and pre-regulated structure, whilst achieving a power supply rejection ratio (PSRR) of -82 dB;The third pW-class circuit employs power supply noise suppression techniques to comprehensively improve the power supply rejection ratio (PSRR) to better than -80 dB across the 100 MHz bandwidth at a power consumption of just 67 pW, with a peak value of -162 dB at 79.4 kHz, and a minimum operating voltage as low as 0.45 V.Sun Xuan (2023) [3] also focused on low-voltage, low-power scenarios. The CMOS reference voltage source proposed by the author consists solely of three PMOS transistors operating in the sub-threshold region connected in series. By utilising the threshold voltage modulation effect related to

ISSN: 2664-9640

channel width and self-bias,the circuit simultaneously achieves process and temperature compensation. With a minimum supply voltage of 0.5 V, the power consumption is merely 500 pW, and in tests involving 16 chips, an on-chip accuracy of 0.57% and an overall PVT relative error of 2.23% were achieved.Zhou Shuang and Chen Xinwei (2019) [4], addressing the impact of reduced drain potential barrier and gate-to-drain leakage on the supply rejection ratio of traditional picoampere-level voltage reference sources, designed a 0.18 μm CMOS self-regulating five-transistor voltage reference source. Its current consumption is only 59 pA, and the supply rejection ratio reaches -62 dB at 100 Hz.Chouhan and Halonen (2017) [5] proposed a scheme utilising a PTAT current-compensating diode connected to the threshold voltage of an nMOSFET, achieving a total current of 115.4 nA and a temperature coefficient of 67 ppm/°C in a 0.18 μm process.In terms of current references, Gagliardi et al. (2025) [6] proposed a novel all-CMOS current reference that utilises the inverse short-channel effect and the narrow-channel effect to achieve first-order temperature compensation based on the geometric dependence of the threshold voltage, outputting 141 nA of current with a single core and a total power consumption of 377 nW.Fassio et al. (2021) [7], on the other hand, focused on power utilisation; their current reference limits the power absorbed by peripheral circuits to 0.1% of the total power across a wide supply voltage range of 0.6 to 1.8 V, achieving nearly 100% power utilisation, thereby paving the way for the widespread deployment of local references on-chip.The above studies indicate that the power consumption of all-CMOS reference sources has been reduced to the pW level; however, most validations are still based on limited laboratory samples, and reliability data regarding batch consistency and long-term drift remain to be supplemented.

2.2. RF Front-End Circuits

The RF front-end is one of the primary power-consuming modules in IoT transceivers; the key to low-power design lies in reducing the supply voltage and bias current of low-noise amplifiers and mixers whilst maintaining the required noise figure and linearity.Tiwari and Mukherjee (2021) [8] proposed a broadband balun low-noise amplifier with no inductors, utilising an nMOS-pMOS configuration to achieve transconductance multiplication.The circuit employs a capacitive-coupled load to resolve the trade-off between voltage gain and voltage margin, and utilises a common-source–common-gate stage to cancel noise. Operating at 0.18 μm process technology, it consumes only 3 mW of power whilst delivering a maximum gain of 19.6 dB and a minimum noise figure of 3.6 dB.Sajad et al. (2020) [9], on the other hand, focused on the sensitivity of low-noise amplifiers to variations in process, voltage and temperature under subthreshold bias. Building upon a common-source, common-gate configuration, they introduced forward body bias and gm-boosting techniques, and designed a temperature-voltage compensator that generates a constant current by subtracting two PTAT currents, thereby effectively stabilising circuit performance.Cai Liying (2023)[10] designed a high-precision dB-linear variable-gain amplifier and automatic gain control circuit for Sub-GHz multi-standard IoT applications. Through a simplified dB-linear control module, they achieved a gain adjustment range of 62.4 dB with a dB-linear error of only ±0.4 dB and power consumption as low as 0.96 mW; furthermore, they employed dual-mode gain adjustment technology to extend the gain range to 68.2 dB.In earlier work, Mao Fangyu (2015) [11] utilised a parallel common-gate stage to achieve broadband input matching and, in combination with feedforward noise cancellation technology, reduced the power consumption of the low-noise amplifier to 1.44 mW under a 1.2 V supply, with a gain of 11.1 dB and a noise figure of 2.7 dB.Dong Yezhi (2013) [12] introduced a compensation inductor into a narrowband amplifier to partially offset the parasitic capacitance of the transistor, thereby increasing the gain without increasing power consumption.In mixer and down-conversion chains, Tedjini et al. (2019) [13] employed a current-sharing LC VCO to drive a single-balanced switch transconductance mixer, realising a complete down-converter-including an adjustable low-noise amplifier-on a 0.13 μm

ISSN: 2664-9640

CMOS process, with a conversion gain of 27 dB and a total power consumption of just 0.97 mW.Zhou Yan (2019) [14] modified the transconductance stage of a 2.4 GHz Gilbert mixer to enable single-ended-to-differential conversion without additional power consumption, achieving a measured conversion gain exceeding 12 dB with a power consumption of 2.88 mW.Gong Yubo (2019) [15], on the other hand, biased the mixer transconductance stage in the subthreshold region, removed the tail current source, and employed an LC parallel network as the load, reducing power consumption to 0.985 mW under a 1.1 V supply.Meng Fanzhen et al. (2017) [16] designed a filtered undersampler that utilises a passive sampling switch and a resonant load at the output of a balun low-noise amplifier to form a bandpass filter, downconverting a 780 MHz RF signal at a sampling frequency of 41 MHz with a total current consumption of only 1.6 mA.In the realm of passive RF front-ends, Purushothaman et al. (2019) [17] proposed a mixer-first architecture utilising implicit stacking of N-path filter substrate capacitance, achieving 13 dB voltage gain and an out-of-band IIP3 of up to +25 dBm with a power consumption of 600 μW on a 22 nm FDSOI process.Zhang et al. (2022) [18], also targeting the Sub-GHz band, demonstrated a fully integrated wide dynamic range receive front-end with an area of just 0.37 mm^2, completely eliminating the need for off-chip matching components, thereby achieving further improvements in compactness and low power consumption.These results indicate that the power consumption of individual RF functional modules has generally entered the milliwatt or even sub-milliwatt range; however, when different modules are combined to form a complete receive chain, inter-stage matching and power domain isolation still introduce additional power overhead.

2.3. Power Amplifiers

The power amplifier is the bottleneck module that determines the overall energy efficiency of the transmit chain; the implementation of high-efficiency power amplifiers using CMOS processes is particularly important for extending the battery life of IoT nodes.Qian Yongxue et al. (2018) [19] developed the world's first all-CMOS RF front-end module for NB-IoT, integrating an RF power amplifier and a controller. Based on proprietary technologies such as Smart-Power and Dynamic-bias, it meets 3GPP power and performance requirements at an ultra-low voltage of 1.8 V, whilst featuring an ultra-low standby leakage current of 0.1 μA, significantly extending the device's standby time.Zhao Kangjie (2021) [20] designed a 2.4 GHz Class-E power amplifier based on a 22 nm SOI process, employing a two-stage amplification structure with differential input and single-ended output. With a total power consumption of only 7.9 mW, it achieved a maximum output power of 4.9 dBm and a peak power added efficiency of 41.5%.Cui Jianhui et al. (2013) [21], addressing the requirements of multi-band IoT applications, proposed a dual-band impedance matching network that does not require switching, and applied it to a Class-D RF power amplifier. This design achieved output powers of 14 dBm and 15.4 dBm at 400 MHz and 600 MHz, respectively, with power added efficiencies of approximately 35% and 34%.Mao Fangyu (2015) [11] incorporated a DC-DC step-down converter and a variable output impedance matching network into the transmitter design, enabling the power amplifier to maintain high efficiency across a wide output power range by adjusting the supply voltage and load impedance.Gong Yubo (2019) [15], based on the SiGe BiCMOS process, employed a five-layer transistor stacking structure to increase the output voltage swing, achieving an output power of 28.1 dBm and a power added efficiency of over 41% in the IoT frequency band, whilst utilising RC feedback to enhance stability.At the transmitter circuit level, Nishio et al. (2020) [22] addressed the issue of power supply voltage fluctuations in low-power biosensing platforms by proposing an inductively coupled transmitter with an auxiliary drive switch; by adaptively controlling the drive transistor under varying supply voltages, they achieved near-constant transmission power.Xu et al. (2020) [23], on the other hand, were the first to propose an inductively coupled transceiver based on bit error rate modulation. By utilising dynamic intermediate interference control technology, they achieved

ISSN: 2664-9640

communication with a transmitter power consumption of 0.3 μW, providing a new approach for ultra-low-power body area networks.Overall, CMOS power amplifiers have achieved efficiencies exceeding 40% at power consumption levels of a few milliwatts; however, most designs remain geared towards single-band, narrowband applications. When addressing the requirements of multi-mode, multi-frequency IoT applications, reconciling broadband linearity with high efficiency remains a major challenge.

2.4. Transceiver Systems and Digital Auxiliary Circuits

The design of a receiver system requires striking an optimal balance between sensitivity, interference immunity and overall power consumption, with the choice of architecture and process technology playing a decisive role. Nam Seog Kim (2025)[24] proposed a CMOS receiver for the 2.4 GHz Bluetooth Low Energy standard. Its key feature is the use of a quadrature bandpass continuous-time ΔΣ analogue-to-digital converter, which, operating at 28 nm, achieves a sensitivity of −95 dBm and an image rejection ratio of 54.2 dBc whilst dissipating only 4.08 mW of total power, whilst also achieving an energy efficiency of 103.2 fJ per conversion step.In her research on low-power receivers, Cai Liying (2023) [10] not only realised an improved low-noise amplifier and passive mixer featuring sub-threshold bias and current sharing structures, but also integrated an RF energy harvesting circuit for self-powered operation of the transceiver, thereby enhancing the system's endurance by tapping into the energy source itself.Meng Fanzhen (2013) [25] employed a simple, zero-IF envelope detection architecture to realise a 780 MHz ultra-low-power receiver on 65 nm CMOS. At a data rate of 20 MHz and a bit error rate of 0.001, the receiver achieved a sensitivity of −65 dBm with a total power consumption of just 4.2 mW.Qiu Wanwei (2019) [26] designed wake-up circuits and RF front-ends for the 5 GHz and NFC bands respectively. The wake-up circuit achieved a trigger sensitivity of −80 dBm with a static current of 3 μA, whilst the NFC receiver attained a sensitivity of 5 mV and a dynamic range of 34 dB with a dynamic current of 3.3 mA, fully demonstrating the contribution of on-demand wake-up to reducing average power consumption.In the area of frequency synthesizers, Zhang Kun (2012) [27] completed the design of integer and fractional phase-locked loops (PLLs) for the 2.4 GHz band based on a 0.18 μm CMOS process. Following optimisation, the voltage-controlled oscillator (VCO) achieved phase noise as low as −123.4 dBc/Hz at 1 MHz, with a lock time of less than 20 μs, whilst keeping the overall power consumption below 15 mW.Haddad et al. (2019) [28], on the other hand, utilised active inductors to replace on-chip spiral inductors, designing a reconfigurable RF VCO with an area of just 54 × 59 μm^2, covering a frequency range from 1.22 to 2.6 GHz.Furthermore, Vivek and Mansi (2023) [29] proposed an inverter-cascode transimpedance amplifier with active feedback, achieving 53.2 dB gain and a 9.2 GHz bandwidth with a power consumption of 3.2 mW under a 1 V supply, providing a low-power reference for broadband optical communication front-ends.The aforementioned system-on-chip (SoC) demonstrations show that, through architectural innovation and advanced process scaling, the total power consumption of the receive chain can now be reduced to a few milliwatts; however, in high-interference scenarios, the linearity and block tolerance of the receiver still often rely on off-chip filter compensation, posing a challenge to full integration.

2.5. Digital Modules and Security Circuits

The normal operation of IoT nodes also relies on the support of low-power digital circuits and security hardware; in particular, minimising the static and dynamic power consumption of the digital section is crucial during sleep and intermittent operating modes.Juveria et al. (2025) [30] designed a negative-edge-triggered true monophase clock D-flipflop using a 7 nm FinFET process. By leveraging the temperature inversion effect inherent to FinFETs, they achieved an extremely low delay of 12.72 ps and a power consumption of 0.86 μW at 300 K, representing a significant performance improvement over 22 nm CMOS;Their team also reviewed the trade-

ISSN: 2664-9640

offs between various advanced trigger architectures in terms of performance, power consumption and bias temperature instability [31], providing a basis for selecting timing units in AI and IoT applications. In terms of hardware security, physical unclonable functions are regarded as ideal primitives for IoT device authentication due to their lightweight nature, but dynamic power consumption has historically constrained their application.Liu and Takahashi (2025) [32] proposed an adiabatic PCF circuit comprising only six transistors, utilising a trapezoidal power clock to achieve energy recovery; it was simulated in 0.18 μm CMOS and demonstrated excellent key characteristics.Monteiro and Takahashi (2021) [33], on the other hand, designed a biphasic clock adiabatic PCF that ensures stable generation of challenge-response pairs through a constant-current charge-discharge strategy and static CMOS logic, whilst thoroughly investigating the effects of body effects and temperature on uniqueness and reliability.In the field of timers, Nishio et al. (2019) [34] implemented a compact, low-frequency gate-leak timer based on differential leakage technology, suitable for use as a wake-up clock source during long periods of hibernation.At a higher level of integration, Hu Jin et al. (2019) [35], utilising a 55 nm CMOS process and the RISC-V open-source processor architecture, integrated a CMOS image sensor interface with an improved asynchronous FIFO synchronisation module to realise a micro-image acquisition system operating at 24.4 mW power consumption, demonstrating the system-level platform's capability to support multi-module collaborative power reduction.Gu Tiejiao (2019) [36] investigated dynamic power management and dynamic voltage scaling algorithms at the operating system level, proposing a process-set-oriented RD-LEDF scheduling strategy and optimising task sequencing in conjunction with a battery discharge model, thereby further exploiting the power-saving potential of IoT nodes at the software layer.The aforementioned work indicates that low-power design has extended from the analogue domain to the digital domain and system level. Adiabatic logic and near-threshold design are gradually addressing the energy consumption bottlenecks in digital circuits; however, the generation and allocation of non-traditional power clocks introduce new complexities into system design.

2.6. Power Management and Energy Harvesting

Power management and energy harvesting are the cornerstones upon which self-powered IoT nodes rely for long-term, maintenance-free operation. Their core lies in the management of nanoampere-level static current and the improvement of voltage conversion efficiency across a wide input range. Wang Kai (2023)[37] designed a solar-powered IoT node chip based on standard CMOS processes, integrating on-chip modules such as a P+/N-well photovoltaic cell, a four-stage low-power charge pump, an energy management unit, and a low-power SAR ADC. This enables the system to operate in duty-cycle mode under solar input, with the charge pump capable of boosting an input voltage of 0.4 V to over 1.25 V whilst consuming less than 0.5 μA.Chen Junxiao (2019) [38] conducted an in-depth study on the design methods for nanoampere-level general-purpose analogue circuits. He proposed a 'floating isolation' protection ring to suppress minority carrier injection interference from the switching power supply power stage into ultra-low-power circuits, and adopted an adaptive bias pulse frequency modulation mode, reducing the buck converter's own quiescent current to just 95 nA whilst maintaining a conversion efficiency of 79.8% under a 2 μA load.Zhang Jidong (2023) [39], in RF-powered passive IoT nodes, utilised diodes connected to MOSFETs to replace passive resistors in forming the LDO feedback network, thereby achieving nanoampere-level leakage current whilst saving layout area, and added phase lead compensation to ensure loop stability;He also designed a 320 kHz ultra-low-power clock circuit capable of being calibrated to a frequency error of ±3%, and a dual voltage-controlled oscillator-type temperature sensor with an accuracy of ±1°C. These studies treat energy harvesting, voltage regulation, bias reference and sensor interfaces as an integrated whole for collaborative design, effectively reducing the system's total quiescent power consumption.However, most power management

ISSN: 2664-9640

solutions remain optimised for specific energy harvesting methods and operating modes; further investigation is required regarding adaptability and reliable startup in complex environments when there are significant variations in the input energy source and load dynamic range.

Beyond solar and RF energy harvesting, thermoelectric and piezoelectric energy harvesting have also attracted increasing attention for self-powered IoT systems because of their ability to exploit environmental energy sources under specific operating conditions. Thermoelectric energy harvesting converts temperature gradients into electrical energy through the Seebeck effect and is particularly suitable for wearable devices, industrial monitoring systems and body-area networks where stable temperature differences exist. However, thermoelectric generators generally provide low output voltages, often in the tens to hundreds of millivolts range, requiring ultra-low-voltage startup circuits, high-gain DC–DC boost converters and maximum power point tracking (MPPT) mechanisms to enable effective energy extraction under weak-input conditions.

Piezoelectric energy harvesting, by contrast, converts ambient mechanical vibration, strain or motion into electrical energy and is widely applied in structural health monitoring, industrial sensing and wearable electronics. Piezoelectric harvesters usually generate high-output-impedance AC signals with large amplitude variations, making rectification efficiency and impedance matching the primary design challenges. Consequently, power management circuits for piezoelectric systems often incorporate active or synchronous rectifiers, impedance matching networks and adaptive energy extraction circuits to maximize harvested power while minimizing switching losses.

Different energy harvesting approaches impose substantially different requirements on power management circuit architectures. Solar harvesting systems primarily emphasize high conversion efficiency under variable illumination conditions and typically employ MPPT-assisted charge pumps or switched-capacitor converters. RF-powered systems focus on ultra-low startup voltage and minimizing leakage current because of extremely limited available input power. Thermoelectric harvesting requires highly efficient boost conversion and cold-start capability at ultra-low voltages, whereas piezoelectric systems place greater emphasis on AC–DC conversion efficiency and dynamic impedance adaptation. Therefore, future ultra-low-power CMOS IoT nodes are likely to adopt energy-aware and reconfigurable power management architectures capable of dynamically adapting to multiple energy sources and operating environments.

2.7. System-Level Integration Challenges

Although significant progress has been achieved in reducing the power consumption of individual functional modules, translating module-level optimization into practical ultra-low-power IoT systems remains a major challenge. In many cases, the total system energy consumption is not simply the sum of each module's standalone power consumption; rather, system-level interactions introduce additional overheads that are difficult to capture during isolated circuit optimization.

One important challenge is power-domain isolation among heterogeneous modules. Ultra-low-power reference circuits, RF front-ends, digital controllers and power management blocks often operate under different voltage domains and duty cycles. Improper power-domain partitioning may lead to leakage current paths, increased standby consumption and unstable operation during mode transitions. Therefore, techniques such as multi-domain power gating, dynamic voltage scaling and adaptive power switching networks have become increasingly important for reducing cross-domain energy overhead.

Noise coupling also becomes more severe as system integration density increases. Switching noise from digital logic, charge pumps and DC–DC converters can couple into ultra-sensitive

ISSN: 2664-9640

analogue blocks through shared substrates, supply rails and interconnect parasitics, degrading the performance of voltage references, low-noise amplifiers and sensor interfaces. Isolation structures, guard rings, differential architectures and dedicated supply routing are therefore often required to suppress substrate and supply noise propagation.

Another critical issue involves startup sequencing and system coordination. Energy-harvesting-powered nodes frequently operate under intermittent and unstable supply conditions, making startup management particularly difficult. Reference circuits, clocks, regulators and digital controllers may require strict activation order to avoid latch-up, unstable bias conditions or repeated cold-start failures. Consequently, low-power systems increasingly employ hierarchical startup control and adaptive wake-up strategies to ensure reliable operation under varying energy availability.

Interface compatibility between modules further limits overall integration efficiency. The mismatch in voltage levels, impedance characteristics, timing requirements and signal formats between analogue front-ends, RF circuits and digital processing units often requires additional interface circuitry, introducing extra power and area overhead. As process scaling continues and heterogeneous integration becomes more common, co-design methodologies that jointly optimize interfaces, architecture and circuit implementation will become essential.

Overall, the gap between module-level optimization and system-level implementation remains one of the key barriers preventing the realization of fully integrated ultra-low-power IoT systems. Future research should therefore move beyond isolated circuit optimization toward collaborative design methodologies that simultaneously consider energy efficiency, robustness and integration complexity.

3. Conclusion

In summary, current CMOS-based low-power circuit design for the Internet of Things (IoT) has demonstrated several distinct characteristics and trends: in terms of technical approaches, through the abandonment of BJTs, the utilisation of the MOS subthreshold region, and the introduction of topological innovations such as inductorless and thermally isolated logic, the power consumption metrics of various functional modules have continued to decrease from the early milliwatt range to the nanowatt and even picowatt levels;In terms of application coverage, low-power design now spans the entire signal chain of IoT nodes, from reference sources and RF transceiver links to power management and digital security modules; regarding process evolution, widespread implementation from 0.18 μm to 7 nm FinFET demonstrates that the inherent speed and power consumption advantages brought by process scaling are being fully utilised.However, existing research still has several shortcomings. Firstly, most literature focuses on the performance limits of individual modules, lacking collaborative design verification that integrates ultra-low-power reference circuits, RF front-ends, power management and digital control into a complete system; system-level issues such as power domain isolation between modules, noise coupling and start-up sequencing require further investigation.Secondly, whilst some circuits have achieved extremely low power consumption in simulations or a small number of laboratory prototypes, data on their robustness and mass-production consistency under the combined effects of PVT variations, electromagnetic interference and long-term ageing remains relatively scarce.Furthermore, subthreshold or adiabatic designs adopted in the pursuit of extreme power efficiency often require dedicated peripheral biasing or specialised power clocks, which in turn increases the complexity of system integration.

ISSN: 2664-9640

References

[1] Pallavi, R., Nayana, D. K., & Sudharshan, K. M. (2026). A low-power, high-stability CMOS bandgap reference with post-regulation for wearable IoT applications. Results in Engineering, 30.

[2] Yang, J. (2023). Research and design of a full-CMOS voltage reference circuit for passive IoT nodes [Unpublished master's thesis]. Guangzhou University. [In Chinese.]

[3] Sun, X. (2023). Design of a process-compensated low-voltage low-power CMOS bandgap voltage reference [Unpublished master's thesis]. University of Science and Technology of China. [In Chinese.]

[4] Zhou, S., & Chen, X. (2019). A pico-ampere CMOS voltage reference for IoT chips. Application of Electronic Technique, 45(11), 42–46. [In Chinese.]

[5] Chouhan, S. S., & Halonen, K. (2017). A 139 nW, 67 ppm/°C BJT-CMOS-based voltage reference circuit. Circuits, Systems, and Signal Processing, 36(12).

[6] Gagliardi, F., Ria, A., Piotto, M., & Bruschi, P. (2025). A CMOS current reference with novel temperature compensation based on geometry-dependent threshold voltage effects. Electronics, 14(13).

[7] Fassio, L., Lin, L., De Rose, R., et al. (2021). A 0.6-to-1.8 V CMOS current reference with near-100% power utilization. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(9).

[8] Tiwari, S., & Mukherjee, J. (2021). An inductorless wideband Gm-boosted balun LNA with nMOS-pMOS configuration and capacitively coupled loads for sub-GHz IoT applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(10).

[9] Nejadhasan, S., Zaheri, F., Abiri, E., & Salehi, M. R. (2020). PVT-compensated low-voltage and low-power CMOS LNA for IoT applications. International Journal of RF and Microwave Computer-Aided Engineering, 30(11).

[10] Cai, L. (2023). Research on key technologies of self-powered low-power CMOS receivers for the Internet of Things [Unpublished master's thesis]. Zhejiang University. [In Chinese.]

[11] Mao, F. (2015). Design of a 780 MHz CMOS low-power high-efficiency RF module for IoT wireless transmission nodes [Unpublished master's thesis]. University of Electronic Science and Technology of China. [In Chinese.]

[12] Dong, Y. (2013). Research and design of a low-noise amplifier for RF front-end of IoT and wireless sensor networks [Unpublished master's thesis]. National Ocean Technology Center. [In Chinese.]

[13] Tedjini, S. A., Slimane, A., Ghorbel, I., et al. (2019). Sub-mW cognitive CMOS frequency down-converter for Internet of Things. IET Microwaves, Antennas & Propagation, 13(12).

[14] Zhou, Y. (2019). Design of a down-converter and quadrature output voltage-controlled oscillator for IoT applications [Unpublished master's thesis]. Soochow University. [In Chinese.]

[15] Gong, Y. (2019). Research on silicon-based power amplifier and low-power mixer [Unpublished master's thesis]. University of Electronic Science and Technology of China. [In Chinese.]

[16] Meng, F., Liu, H., Wang, M., et al. (2017). Design of a CMOS low-power undersampling filter for IoT. Journal of Xidian University, 44(3), 108–113. [In Chinese.]

[17] Purushothaman, V. K., Klumperink, E. A. M., Clavera, B. T., & Nauta, B. (2019). A fully passive RF front end with 13-dB gain exploiting implicit capacitive stacking in a bottom-plate N-path filter/mixer. IEEE Journal of Solid-State Circuits, 55(5).

[18] Zhang, Y., Liu, B., Someya, T., et al. (2022). A 0.37 mm^2 fully-integrated wide dynamic range sub-GHz receiver front-end without off-chip matching components. IEICE Transactions on Electronics, E105C(7).

[19] Qian, Y., Meng, H., Peng, F., et al. (2018). Low-power RF front-end for NB-IoT based on CMOS technology [Technical report]. Beijing Zhongke Hantianxia Electronic Technology Co., Ltd. [In Chinese.]

[20] Zhao, K. (2021). Design of a 2.4 GHz low-power power amplifier for the Internet of Things. Application of IC, 38(12), 10–12. [In Chinese.]

ISSN: 2664-9640

[21] Cui, J., Zhang, K., & Tian, T. (2013). Design of a dual-band RF class-D power amplifier for the Internet of Things. Microelectronics & Computer, 30(12), 129–132. [In Chinese.]

[22] Nishio, Y., Kobayashi, A., & Niitsu, K. (2020). Low-power inductive-coupling transmitter using supply-insensitive auxiliary driving switch under supply-voltage fluctuation. Sensors and Materials, 32(8).

[23] Xu, G., Hayashi, K., Arata, S., et al. (2020). Design and theoretical analysis of bit error rate (BER)-modulated inductive-coupling transceiver using dynamic intermediate interference control technique for low-power communication. Sensors and Materials, 32(8).

[24] Kim, N. S. (2025). A low-power complementary metal-oxide-semiconductor receiver with quadrature bandpass continuous-time delta–sigma analog-to-digital converter for IoT applications. Sensors, 25(6).

[25] Meng, F. (2013). Design of a 780 MHz CMOS ultra-low power receiver for IoT wireless nodes [Unpublished master's thesis]. University of Electronic Science and Technology of China. [In Chinese.]

[26] Qiu, W. (2019). Design of CMOS ultra-low power RF front-end system for IoT applications [Unpublished master's thesis]. Shenzhen University. [In Chinese.]

[27] Zhang, K. (2012). Design of an RF SoC for the Internet of Things [Unpublished master's thesis]. Beijing Jiaotong University. [In Chinese.]

[28] Haddad, F., Ghorbel, I., & Rahajandraibe, W. (2019). Design of reconfigurable inductorless RF VCO in 130 nm CMOS. BioNanoScience, 9(2).

[29] Niranjan, V., & Jhamb, M. (2023). Design of a low-power 180 nm broadband CMOS transimpedance amplifier for bio-medical & IoT applications. International Journal of Information Technology, 15(5).

[30] Juveria, S. H., Shashank, R., Panigrahy, A. K., & Ajayan, J. (2025). Thermal dynamics of 7-nm FinFET process-based negative edge triggered (NET) TSPC D flip-flop for future AI and IoT applications. Journal of the Korean Physical Society, 88(3).

[31] Juveria, S. H., Shashank, R., Ajayan, J., et al. (2025). A review of performance and reliability issues in D flip-flops for future artificial intelligence and Internet of Things applications. IET Circuits, Devices & Systems, 2025(1).

[32] Liu, J., & Takahashi, Y. (2025). Design and simulation of low-power adiabatic PUF circuit. Electronics, 14(22).

[33] Monteiro, C., & Takahashi, Y. (2021). Low-power two-phase clocking adiabatic PUF circuit. Electronics, 10(11).

[34] Nishio, Y., Kobayashi, A., & Niitsu, K. (2019). Design and calibration of a small-footprint, low-frequency, and low-power gate leakage timer using differential leakage technique. IEICE Transactions on Electronics, E102.C(4).

[35] Hu, J., Xie, L., Zou, W., et al. (2019). Design of a miniature image acquisition system based on low-power SoC. Journal of Hunan University (Natural Sciences), 46(2), 86–91. [In Chinese.]

[36] Gu, T. (2019). Research on low-power optimization technology for Internet of Things [Unpublished master's thesis]. Beijing University of Posts and Telecommunications. [In Chinese.]

[37] Wang, K. (2023). Design of low-power light-sensing IoT node chip based on CMOS process [Unpublished master's thesis]. Xidian University. [In Chinese.]

[38] Chen, J. (2019). Research and implementation of key technologies for ultra-low power on-chip power management for self-powered IoT nodes [Unpublished master's thesis]. Zhejiang University. [In Chinese.]

[39] Zhang, J. (2023). Design and implementation of an ultra-low power analog front-end for passive IoT nodes [Unpublished master's thesis]. Xidian University. [In Chinese.]