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The Evolution of Logic Device Technology in the Post-Moore's Law Era: From Advanced CMOS to Carbon-Based Transistors

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Abstract

As integrated circuit manufacturing processes continue to advance towards the nanoscale, the traditional development model of CMOS devices-which relies on scale-down to enhance performance-is increasingly being constrained by factors such as the short-channel effect, rising power consumption, and material performance limitations. The continued evolution of Moore's Law thus faces new challenges. The development of logic devices in the post-Moore's Law era is gradually shifting from a focus solely on scaling down to a combined approach involving the optimisation of device structures and the exploration of new materials. On the one hand, advanced CMOS continues the development of silicon-based logic technology by enhancing gate control capabilities and integration density through structural innovations such as FinFETs, gate-all-around(GAA)transistors, and complementary field-effect transistors(CFETs); on the other hand, carbon nanotube field-effect transistors(CNTFETs), with their excellent carrier transport properties and the advantages of nanoscale electrostatic control, offer new possibilities for overcoming the scaling limitations of traditional silicon-based devices. This paper focuses on the technological evolution of logic devices in the post-Moore's Law era, analysing the transition of advanced CMOS devices from two-dimensional to three-dimensional structures and the limitations encountered, whilst further discussing the current status and key challenges facing carbon nanotube materials, CNTFET devices, and carbon-based logic integration. Through a comparison of these two technological pathways, this paper concludes that the future development of logic devices will not involve replacing one technology with another, but will instead follow a trend of continuous optimisation of advanced CMOS alongside the synergistic development of new material-based devices.

Keywords

Post-Moore's Law Era; Advanced CMOS; Carbon Nanotube Field-effect Transistors; Logic Devices; Monolithic Three-dimensional Integration.

1. Introduction

Moore's Law has been central to the very fast growth of the integrated circuit industry over many decades[1]. It is the continuous miniaturisation of transistor sizes that makes higher chip integration feasible, enables more computing power, and lowers the average cost of computation. During the conventional scaling era, Dennard's scaling rule meant that smaller transistors operated at lower voltages and with less power density; as a result, the trend toward miniaturisation dominated-as a single factor-the development of semiconductor technology.

However, as transistors have entered the nanoscale, traditional planar CMOS structures are gradually approaching their physical limits[2,3]. As the channel length continues to decrease, the gate's ability to control the channel potential diminishes, and issues such as the short-

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channel effect, a reduction in the drain-induced potential barrier, and increased drain current are becoming increasingly prominent. At the same time, as the number of transistors continues to increase, power consumption, heat dissipation, and manufacturing costs have also become significant factors limiting the further development of integrated circuits. Consequently, the future development of logic devices can no longer rely solely on size reduction, but must instead achieve performance improvements through new structural designs and material systems. In response to the technological challenges of the post-Moore ' s Law era, current research into logic devices has primarily taken two complementary development paths. The first path involves structural innovation within the existing silicon-based CMOS framework, improving gate control capability by enhancing the three-dimensional features of the devices. From FinFETs to GAA and on to CFETs, advanced CMOS continues to optimise transistor structures to sustain the developmental advantages of silicon-based technology. The second approach involves exploring novel channel materials; by introducing low-dimensional materials with superior transport properties, it aims to overcome the limitations of traditional silicon devices at the level of intrinsic material properties.

Among these, carbon nanotubes are regarded as one of the most promising new materials for logic devices in the post-Moore ' s Law era, owing to their one-dimensional structure, high carrier mobility, and excellent electrostatic control capabilities[4,5]. In recent years, with advances in the fabrication of high-purity semiconductor-type carbon nanotubes,wafer-scale alignment techniques, and CNTFET circuit integration technologies, carbon-based logic devices have gradually progressed from fundamental physics research to the system-level validation stage.

The present paper is devoted to a study of logic device technology in the post-Moore ' s law epoch. As illustrated in Figure 1, logic devices now appear to develop mainly-though not exclusively-along two technical paths: optimisation of advanced CMOS geometries or use of carbon-based materials. First, we look at the development of advanced CMOS from a planar standpoint up to three-dimensional forms, as well as at the scaling limits it meets in practice. We then consider progress in carbon nanotube transistors-on the levels of material quality, of circuit design, and of logic layout-and evaluate the principal obstacles to full industrial deployment. Finally, having compared the two technical approaches, we consider their likely future roles in logic systems, which may come about thanks to joint advances in structure, in materials, and in three-dimensional integration.

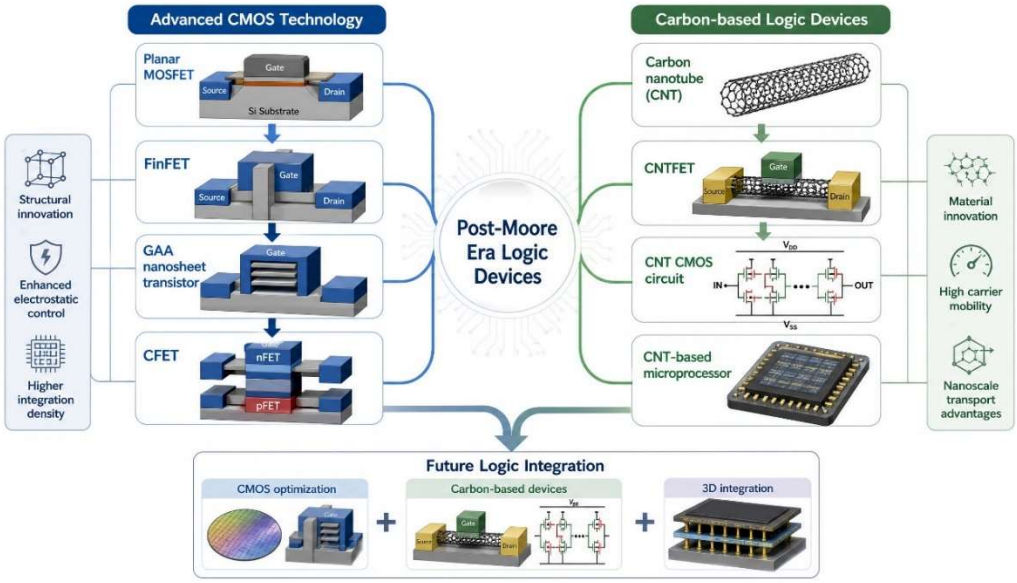


Figure 1. Evolution roadmap of logic devices in the post-Moore era.

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2. Evolution of Advanced CMOS Logic Devices

2.1. Challenges Facing CMOS Scaling in the Post-Moore's Law Era

To date, improvements in integrated circuit performance have been largely based on the shrinking of transistor dimensions. However, with the advent of nanoscale devices, the growth of standard planar MOSFETs is coming increasingly under physical restrictions of various kinds. As the channel length keeps getting smaller, the effect of the source and of the drain on the channel's potential rises, thereby complicating gate control of the charge carriers. This gives rise to phenomena such as short-channel effects, leakage currents, and higher energy consumption.

By now it is clear that CMOS technology-after the Moore's Law epoch-must no longer be considered solely as an exercise in shrinking dimensions, but also as one of transistor optimisation. The idea of enlarging the contact area (between gate and channel) to achieve better electrostatic control is one of the main ways of prolonging silicon-based CMOS technology.

Considering technological evolution as a whole, advanced CMOS has been moving away from two-dimensional planar configurations toward three-dimensional forms.FinFETs achieve better gate control by virtue of a three-dimensional channel; GAA fully wraps the channel with the gate, while CFETs take advantage of vertical stacking to greatly increase transistor density. With such progress, it is evident that development of advanced CMOS is not merely about reducing dimensionality but about persistent optimization-of the physical layout and of the device structure itself. Nevertheless, when dimensions fall still further, silicon's own transport-related constraints-as well as the rising intricacy of production-make it hard to push traditional CMOS ahead to highly advanced nodes, and so encourage study of devices based on alternative channel materials.

2.2. FinFET: Three-dimensional Structure Enhances Gate Control Capability

When traditional planar MOSFETs were scaled down to the nanoscale, gate control-i.e., the ability to regulate the charge carriers-became a limiting factor for performance improvement. The idea of FinFETs is basically to change the shape of the channel so that the gate may exert better control over current[6].

About planar MOSFETs, FinFETs employ a channel of a fin-like vertical form, which allows the gate to regulate the channel area in more than one direction, thus eliminating-more or less-short-channel problems and minimizing off-state leakage current. As a result, FinFETs are now an important part of the technological basis for high-performance logic circuits.

The main advantages of FinFETs come not so much from progress in materials as from optimisation of their structure. As devices become smaller-i.e., as they move toward more sophisticated nodes-the fin width cannot be reduced indefinitely due to manufacturing limits, while scattering of carriers and parasitic effects grow slowly but steadily, thereby complicating attainment of both high performance and low power with FinFETs[7,8]. In view of this, improving gate control has now been established as the key goal for new generations of CMOS structures.

2.3. GAA and CFET: Novel CMOS Architectures for Extreme Scaling

To improve gate control at the nanoscale, the Gate-All-Around(GAA) transistor has been proposed. Unlike FinFETs-whose principal method of multi-directional gate control is a fin-like channel-GAA configurations encircle the channel entirely with the gate, and thus allow field action along many directions on the channel region. The electrostatic control is correspondingly good, and short-channel effects are strongly curtailed even at small dimensions.

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The value of GAA is to be seen primarily in its capacity-relative to fin width and to gate-control range-to circumvent the difficulties of continuous scaling in FinFETs.Nanosheet versions of GAA permit an easy adjustment of the balance between drive strength and energy use (via channel width) and hence seem well suited to guide future logic innovations at smaller technology nodes[9]. Yet, even with improved gate control, scaling down the transistor to ever-smaller dimensions still leaves unresolved issues of standard-cell area and of very high integration density.

With GAA as a basis, complementary field-effect transistors(CFETs)now turn to the idea of three-dimensional transistor stacking. As illustrated by Figure 2, recent CMOS transistor designs-originally based on planar MOSFETs-have gone on to use FinFETs or GAA and now CFETs; their main purpose is to maintain steady progress toward smaller logic elements by means of improved gate control and of three-dimensional integration (without loss of performance). Among traditional CMOS structures, it is normal to find nFETs and pFETs laid out horizontally. A vertical arrangement-of complementary transistors as a whole-makes CFETs more compact without loss of CMOS logic or of standard-cell integration density; such an idea is now being taken seriously as one of the main candidates for better area efficiency in later-stage CMOS[10]. Still, CFETs suffer from certain difficulties: complexity of vertical construction, control of uniformity across layers, and handling of thermal budgets.

Generally speaking, FinFETs, GAA, and CFETs are part of a development path by which silicon-based CMOS keeps Moore's Law alive through structural innovation. From FinFETs-whose three-dimensional gate control is now improved-to GAA (with full channel enclosure) and to CFETs (which attempt vertical integration), advanced CMOS has been instrumental in raising the integration density of devices.However, if present-day device dimensions come too close to the actual physical limits of silicon and of its manufacture, optimisation of structure alone may fail to satisfy future needs. Consequently, future progress with logic devices seems to demand not just continuing refinement of CMOS but also investigation of novel channel substances-such as carbon nanotubes-to secure breakthroughs at the materials level.

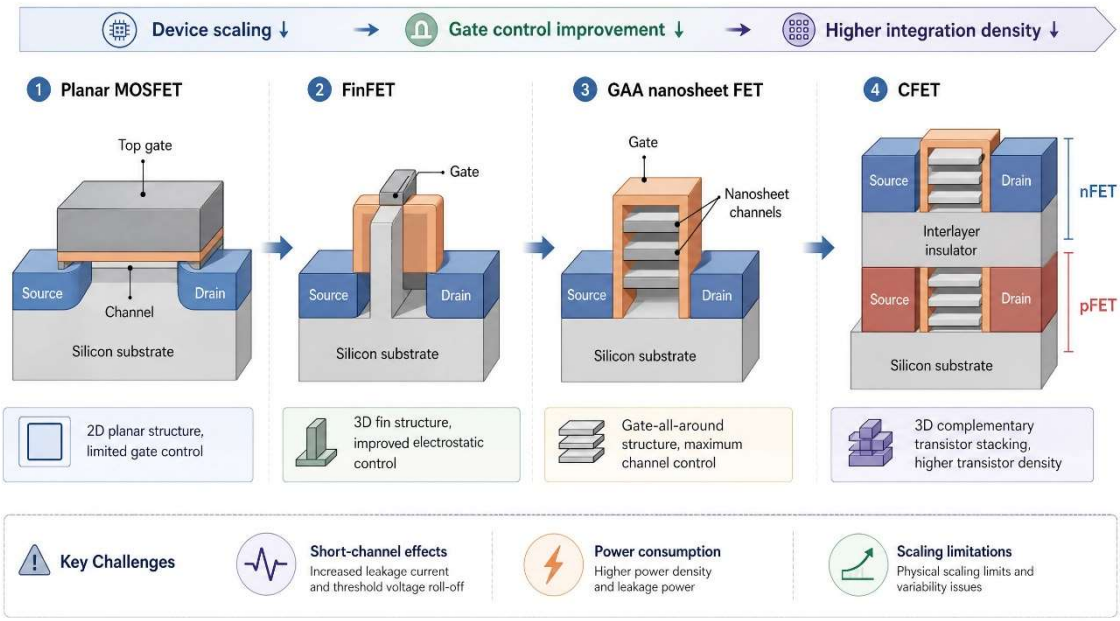


Figure 2. Evolution of advanced CMOS transistor architectures from planar MOSFET to CFET.

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3. Exploration of Carbon-Based Transistor Technologies

3.1. Fundamentals of Carbon Nanotube Materials and Wafer-Scale Fabrication

Carbon nanotubes, as a one-dimensional nanomaterial, are formed by the rolling up of graphene layers[4]. Owing to their unique one-dimensional structure, carbon nanotubes possess excellent carrier transport capabilities and inherent ultra-thin-film characteristics, whilst maintaining good electrostatic control at the nanoscale; they are therefore regarded as key candidate materials for overcoming the scaling limitations of silicon-based CMOS.

The use of carbon nanotubes for large-scale logic integration continues to be hampered by problems of material preparation. Logic circuits depend on great uniformity of the channel material, but there are-as yet-difficulties concerning the metallic fraction of nanotubes, their packing density, and their precise placement when fabricated from carbon. Consequently, the attainment of dense, pure carbon nanotube arrays-uniform across a whole wafer-is central to any industrial attempt at CNT technology.

3.2. CNTFET Device Structure and Key Technologies

Based on high-quality semiconductor-type carbon nanotube arrays, researchers have developed CNTFET devices. Compared with traditional silicon devices, CNTFETs offer potential advantages in terms of scaling and low-power operation, whilst their excellent transport properties open up new possibilities for future high-performance logic computing[11,12].

Though CNTFETs have many advantages, this does not yet justify replacing CMOS with them. Realisation of useful applications still depends on solving several major problems. Among such problems is the contact resistance-between metal and carbon nanotube-which strongly influences the operation of the device and must be handled carefully by contact engineering; at the same time, circuits on a large scale need great uniformity and great dependability of the parts[13].

In addition, carbon-based devices seem to offer definite advantages when it comes to doping. By means of contact materials having various work functions, one may regulate both electron and hole transport, and so design complementary logic systems or reduce-on a nanometer scale-the irregularities caused by ordinary doping techniques (as applied today)[14,15].

3.3. Development of Carbon-Based Logic Integration

During the past few years, CNT technology has advanced-slowly at first-from a study of isolated transistors up to logic circuits and to full system integration[16,17]. Carbon nanotube inverters and logic gates, as well as microprocessor-scale components, have been shown to work; this confirms that logic based on carbon may be of great value for computer applications[18].

About fully mature CMOS processes, CNTFETs continue to face difficulties in becoming industrialised. After many years of study and progress, silicon-based CMOS now has a very well-developed wafer technology, while carbon-based systems still lack uniformity of material quality and of manufacturing integration-along with reliable methods for making large-scale circuits[19].

From a general standpoint, carbon-based technology is more likely to serve as a complement-not necessarily as a replacement-to advanced CMOS in the future. For instance, it might be useful to apply the low-temperature fabrication of carbon nanotubes together with silicon-based CMOS to obtain three-dimensional heterogeneous integration; this possibility seems worth examining in the light of the post-Moore ’ s Law technological landscape.

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4. Summary and Future Outlook

4.1. Summary of Key Research Content

The present paper deals with the development of two technological trends-advanced CMOS and carbon-based transistors-with respect to the course taken by logic-device technology after the arrival of the Moore's Law era. Silicon-based logic devices are now being examined in terms of transistor designs that have evolved from standard planar MOSFETs toward 3D configurations such as FinFETs, GAA, or CFETs.By improving gate control of the channel and by raising the integration density of devices, advanced CMOS methods help to avoid or to minimize the short-channel problem (and its scaling-related consequences), becoming the main technological path along which Moore's Law is kept alive.

About devices based on novel materials, carbon nanotubes are regarded as key candidate materials for overcoming the scaling limitations of traditional silicon-based devices, owing to their one-dimensional structure, high carrier transport capability and excellent electrostatic control properties. In recent years, with advances in the fabrication of high-purity semiconductor-type carbon nanotubes,high-density arraying and the optimisation of CNTFET devices, carbon-based logic devices have gradually progressed from single-transistor research towards logic circuit and system integration.

As a whole, the growth of logic devices after the Moore's Law epoch is characterised by simultaneous progress in ' structural optimisation ' and ' material innovation '.Advanced CMOS still exploits its established industrial strengths thanks to developments of device architecture, and carbon-based transistors may well help to solve-eventually-the physical limits of silicon in present-day use.

4.2. Future Development Directions

Among the prospects for logic devices, two areas seem to dominate: the continuing optimisation of advanced CMOS and the still-growing use of carbon-based transistors. For advanced CMOS, it is safe to assume that three-dimensional and high-density integration will be major trends. New configurations-such as GAA or CFET-that improve the control of transistor gates and the use of available space may help to sustain silicon logic in a form of higher performance going forward.

About carbon-based transistors, research efforts should focus heavily on both improved reliability and mass production methods. On the one hand, the quality of carbon nanotubes has to be pushed forward-to allow fabrication at wafer level with great purity, with many tubes and with regular alignment; on the other hand, contact details, device geometries and integration techniques need improvement if the CNTFET is to go beyond being a laboratory curiosity and become part of real-world technology.

Another promising future development is the integration of carbon-based devices with already established silicon technologies. By means of low-temperature processing-something carbon nanotubes allow-it is feasible to consider heterogeneous integration alongside ordinary CMOS methods, and so to open up an alternative technical possibility for the manufacture of high-density logic circuits in the years ahead.

4.3. Key Challenges and Bottlenecks to Industrialisation

Although carbon-based logic devices hold significant potential for development, their industrialisation still faces several key challenges. Firstly, the consistency of wafer-level material preparation remains a core issue limiting the development of CNT technology. Logic chips require a large number of transistors with highly consistent performance, yet carbon nanotubes remain difficult to control in terms of purity, packing density, and spatial distribution. Therefore, achieving high-quality, large-scale, and uniform CNT array fabrication

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is a crucial foundation for future industrial applications. Secondly, the stability of device performance still needs to be further improved. The contact between carbon nanotubes and metal electrodes, fluctuations in electrical parameters, and variations between devices all affect the reliability of logic circuits. How to reduce device variability and improve the operational stability of large-scale circuits is a problem that must be resolved for CNTFETs to transition from experimental research to industrial manufacturing[20,21]. Consequently, the future development of carbon-based logic devices not only depends on breakthroughs in material performance but also requires the synergistic optimisation of material preparation, device design and manufacturing processes.

5. Conclusion

The era after Moore's Law no longer relies solely on shrinking transistor dimensions to boost chip performance. Instead, device development advances by combining structural upgrades and innovative channel materials. Structural upgrades including FinFET, GAA, and CFET architectures keep improving gate control and transistor density for silicon CMOS, which will remain the mainstream manufacturing choice over the next decade. Carbon nanotube FETs stand out for outstanding carrier mobility and thin-channel geometry, offering a viable way to break silicon's inherent physical scaling limits. Even so, widespread industrial replacement is unrealistic right now. Barriers such as uneven nanotube synthesis, poor process compatibility, and difficulties in mass fabrication still hold back CNTFET commercial rollout. This means we will not see one single technology fully replace another within post-Moore industrial chains. Instead, future logic chips will evolve through three complementary directions: continuous optimization of silicon CMOS, deeper research into carbon-based hardware, and the rise of monolithic 3D heterogeneous integration. Combined progress in these three areas will deliver computing hardware with faster speeds, less power loss, and higher packing density.

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