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Research Progress in Packaging Technology of MEMS Inertial Navigation Micro-system

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Abstract

As the demand for ultra small Micro-Electro-Mechanical System(MEMS) inertial navigation microsystems in intelligent micro air vehicles becomes increasingly urgent, DARPA is investing heavily in the development of Micro Inertial Measurement Unit (MIMU) to enable inertial navigation systems to have higher integration, smaller size, lower power consumption, and lower cost. This article introduces the three-dimensional integration technology of MEMS inertial navigation microsystems, system packaging architecture design, and Through Silicon Via(TSV) vertical interconnect technology of MEMS chips. It analyzes and studies the ways and future development directions of three-dimensional integration of MIMU inertial navigation systems, and proposes solutions and paths to significantly improve the integration degree of MEMS inertial navigation systems.

Keywords

MEMS inertial navigation micro-system; Micro Inertial Measurement Unit(MIMU); 3D integration technology; Through Silicon Via(TSV).

1. INTRODUCTION

As unmanned flights gradually develop in the direction of miniaturization and lightweighting, MEMS inertial navigation systems play an extremely important role, which are characterized by small size, strong overload resistance, high capacity and low cost[1]. In the next step, the MEMS inertial navigation system will be developed towards the goal of using it in micro-nano-satellites, micro-detection vehicles, micro-small ground robots and other micro-intelligent equipment, which requires the use of advanced packaging and integration technology to further reduce the size of the existing MEMS inertial navigation system to 1/5 to 1/10 of the existing level.

At present, the domestic and foreign system packaging integration technology is to use three-dimensional integration technology, from the original 2D to 2.5D and 3D direction[2]. Using three-dimensional integrated manufacturing technology, so that each functional module occupies a layer of chips. High-density TSVs make it possible to integrate chips of different functional types and process materials into a single system. This complex system contains multiple types of circuits such as analog circuits, digital circuits, RF circuits, optical systems, and MEMS micro-mechanical sensors, etc. The development of MEMS inertial navigation systems is reflected in the all-siliconization of MEMS inertial devices, wafer-level vacuum/hazard-tight packaging of the devices, and ASICization of the processing circuits, which enables system-on-a-chip SoC integration of the inertial devices and inertial guidance system-level package SiP integration.

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2. DARPA'S NGIMU PROGRAM

In March 2016, DARPA awarded a $6.27 million contract to Northrop Grumman (Nog) Corporation to develop a next-generation navigation-grade miniature inertial measurement unit (MIMU) based on advanced MEMS technology, which is required to be able to sense acceleration and angular displacement with higher accuracy in a smaller volume than existing IMUs to provide data support for navigation control systems. Under the contract, NORG will develop and validate its MEMS-based gyroscopes and accelerometers to meet the characterization and environmental requirements[3]. If this study is successfully completed, DARPA will also award Nogg $3.5 and $1.84 million, respectively, to conduct the second and third phases of the study, which will include testing the LR-500-specific MEMS IMUs for size, weight, power consumption, and performance parameters, as well as testing a prototype of Nogg's developed MIMUs in a simulated defense environment. The IMU development contract is part of DARPA's Precision Stabilized Inertial Guidance for Navigation-Grade Inertial Measurement Units for Modern Equipment (PRIGM:NGIMU) program. The goal of the program is to develop navigation-grade IMUs that can effectively reduce cost and size, requiring that the advanced MEMS inertial sensors integrated in the IMU have the smallest mass, volume, and power consumption to replace MEMS inertial measurement systems in currently deployed applications. The system specifications are: volume of 82cm^3, weight of 160g, power consumption of less than 3W, operating temperature range of -55°to +85°, system bandwidth of 70Hz, zero-bias stability of 0.01°/h for gyroscopes, and zero-bias stability of 25ug for accelerometers.

DARPA launched the NGIMU series of highly integrated navigation guidance microsystems research program, micro-inertial navigation system integration manufacturing technology is one of the extremely important research direction. The key lies in how to use advanced integrated manufacturing technology to realize the small volume, low cost and high volume production of inertial devices.

3. THREE-DIMENSIONAL INTEGRATION TECHNOLOGY

MEMS inertial navigation system contains MEMS inertial devices and analog, analog-to-digital conversion, data processing, communication interface and other circuits.The way to miniaturize the MEMS inertial navigation system is mainly through the advanced packaging process, the MEMS inertial devices and IC components for packaging integration[4], and its technological pathway from the Multi-Chip-Module (MCM) to the SiP technology, SoC technology, and then to the wafer-level chip packaging(WLCSP) technology, three-dimensional heterogeneous stacked integration technology development, which is shown in Figure 1[5].

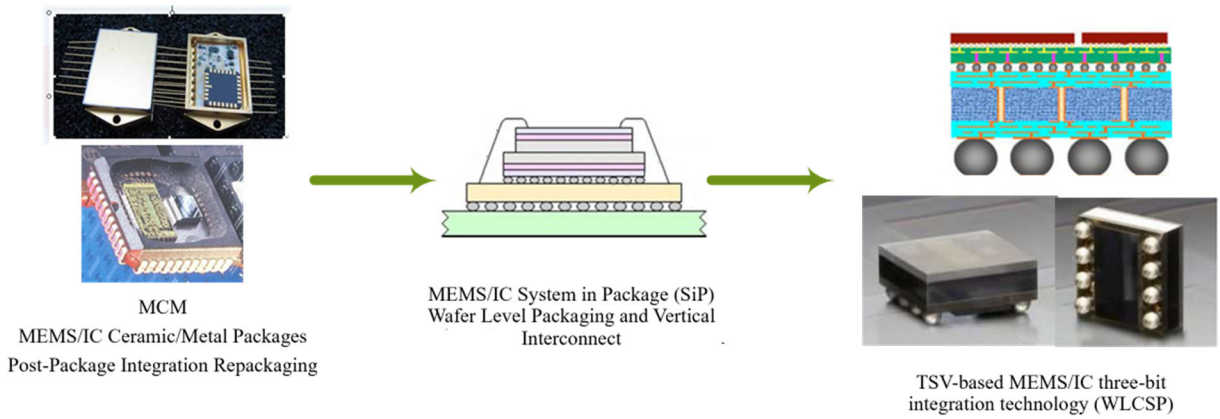

Figure 1. MEMS inertial device packaging technology development

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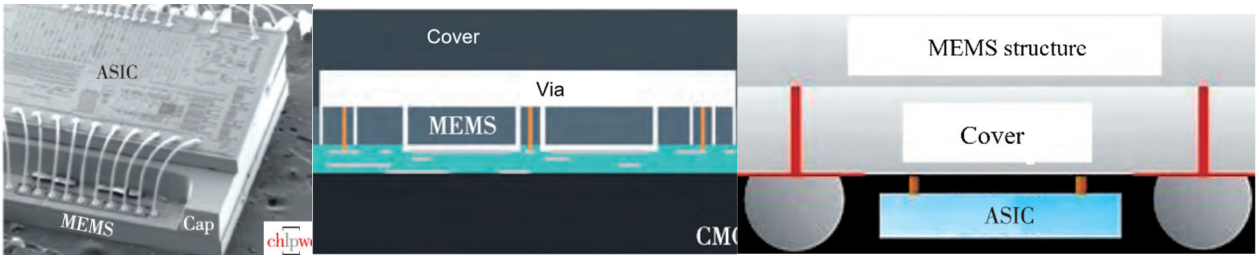
There are three kinds of inertial MEMS 3D integration techniques, as shown in Figure 2: (1) Inertial MEMS chip and MEMS-specific ASIC chip layer stacking, using lead bonding to realize the electrical connection between the two chips. (2) In the manufacturing process, the inertial MEMS wafer and the MEMS-specific integrated circuit IC wafer are both bonded to realize the chip lamination and electrical connection. A package integration technology scheme with lateral electrode leads is usually adopted, where the metal leads in the ASIC are directly used as electrical lead wires across the inside and outside of the package. (3) 3D integration of inertial MEMS based on 3D silicon through-hole interconnect (TSV) technology (e.g., WLCSP technology).



a)Wire Bonding Integratio b)Wafer-level bonding integration c)Based on TSV technology integration

Figure 2. MEMS 3D integration technology

The above three 3D integration methods realize the stacked integration of inertial MEMS chip to chip (C2C), chip to wafer (C2W) and wafer to wafer (W2W) to achieve miniaturization of inertial navigation[6].

4. INERTIAL NAVIGATION MICROSYSTEM ARCHITECTURE

The U.S. DARPA lab's folded chip structure MIMU utilizes two technological solutions, a hexahedral structure and a pyramid structure, as shown in Figure 3. The independent sensors were prepared by silicon on insulating substrate (SOI) process technology, and the 6-axis inertial instruments were distributed on the six sides of the cube, and monolithic integration was realized by flexible connecting boards, and a latch structure for fixing the folded structure was also formed to obtain a 3-dimensional IMU microsystem, which is less than 1 cm3. For the consideration of the mechanical stability of hexahedral structure, the use of resin and solder was also investigated to The effect of reinforcing the folded pyramid was investigated. The former was tested to be within 4mrad of the sensor axis variation, while the latter was improved to be within 0.2mrad. This scheme realizes the monolithic integration of 6-axis IMUs, but this integration scheme limits the preparation process of MEMS instrumentation and processing, while the yield of multi-sensor monolithic integration is low.

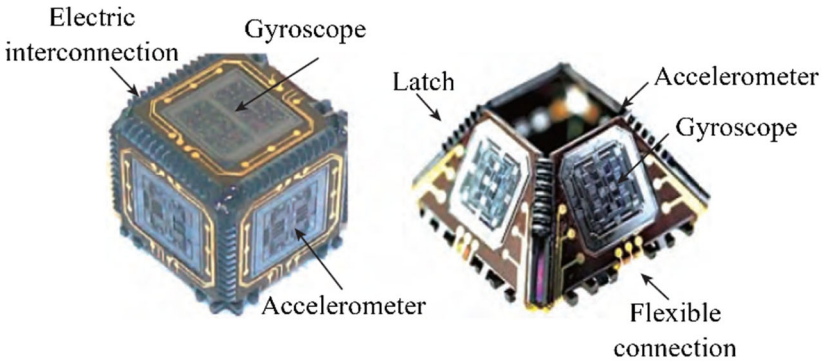


Figure 3. Integrated foldable 6-axis IMU

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The MIMU 3D integration technology based on TSV adapter board from Fraunhofer Institute, Germany, utilizes the TSV adapter board as a common substrate platform, and as shown in Figure 4, a rewiring layer is fabricated on the upper and lower surfaces of the silicon wafer containing TSV interconnections, and microbumps are utilized to assemble an inertial MEMS chip and a MEMS-specific IC chip on the TSV adapter board. The inertial MEMS 3D integration technology based on the TSV adapter board can take advantage of the TSV adapter board's advantages in thermal expansion coefficient mismatch, line width matching, etc[7].It releases the traditional inertial MEMS 3D integration technology's constraints on the MEMS-specific ICs in terms of optional processes, and provides a design space for the low stress assembly of the inertial MEMS chips, allowing the integration of more multi-functional chips with openness features, advantages, as shown in Figure 5. At present, the manufacturing technology has been able to meet the general application requirements, but compared with the 3D integrated manufacturing related to 3D integrated design methodology, device reliability, heat dissipation, multifunctional materials and device integration and other aspects of the needs, there is still a gap. Focusing on these issues, 3D integration technology will be studied in depth in terms of model simulation, design methodology, reliability assessment and improvement, system testability signal design, heat dissipation optimization and efficiency improvement, as well as 3D integrated manufacturing capability, yield and cost control[8].

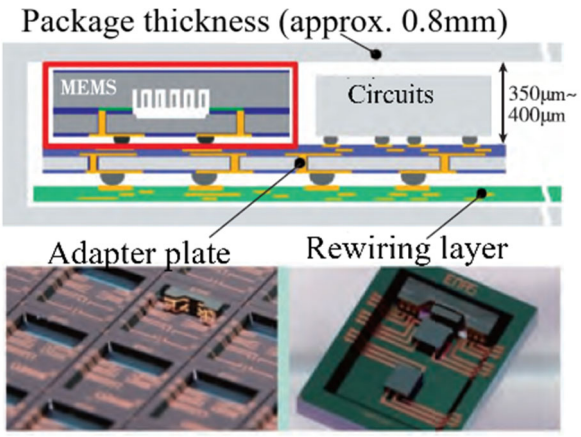

Figure 4. Based on TSV silicon adapter plate integration technology

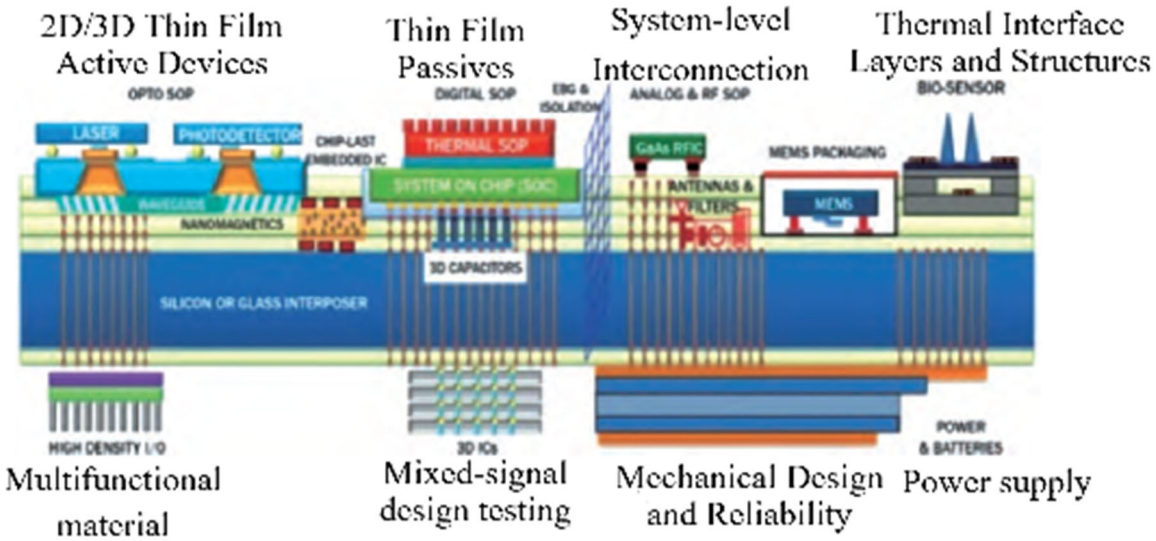

Figure 5. Complex microsystems integration technology based on TSV silicon adapter boards

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5. TSV VERTICAL INTERCONNECT TECHNOLOGY

Since the thickness of the inertial MEMS chip is generally above 300 um, in order to match the mechanical strength of the inertial MEMS chip and the TSV adapter plate, the thickness of the TSV adapter plate usually needs to be greater than or equal to 200 um. At the same time, due to the mismatch of the thermal expansion coefficient of the copper TSV interconnect with the surrounding silicon substrate, the interconnect diameter of the copper TSV is usually controlled to be less than or equal to 20 um and the TSV interconnect The depth-to-width ratio of TSV interconnects is greater than or equal to 10, which is a big challenge for the current TSV technology[9].

In 2012, with the help of glass-melt reflow-based silicon through-hole technology, Silex realized the development of a 2.5D silicon adapter board, in which the aperture diameter of the TSVs for BGA ball implantation is 50 um and the spacing is 150 um. The adapter board solution that also uses low-resistance silicon to realize vertical interconnections is the through-glass through-via (TGV) technology, as shown in Figure 6. This technology adopts a glass-melt process, which is featured with a glass-etched silicon interconnect inside the glass wafer, and the glass-etched silicon interconnect inside the glass wafer. The technology uses a glass melting process, which is characterized by bonding the glass wafer with a silicon wafer etched with silicon pillars, and heating it at high temperature until the glass is molten, so that the silicon pillars are embedded in the glass wafer. The process is relatively less difficult, and the thickness of the adapter plate can be up to 200 um and above. SchottHermes uses this technology to realize the WLCSP integration of MEMS-ICs[10].

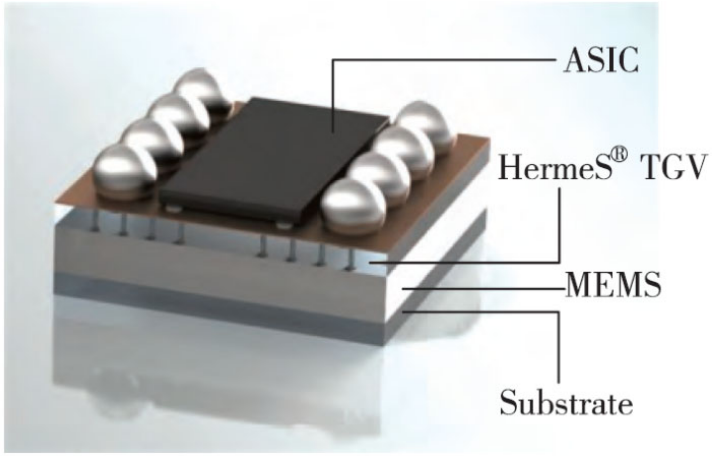

Figure 6. Glass melt backfill TGV vertical interconnect technology

In order to meet the integration needs of different devices, AAC Microtec and Silex in Sweden have developed the metal-through-hole (Met-Via) technology, as shown in Figure 7. It is characterized by the fact that compared with conventional TSVs, this technology can fabricate adapter plates on silicon wafers with a thickness of 300 um to 800 um, and the adapter plates are stiff, which makes them particularly suitable for the three-dimensional integration of stress-sensitive MEMS sensors.

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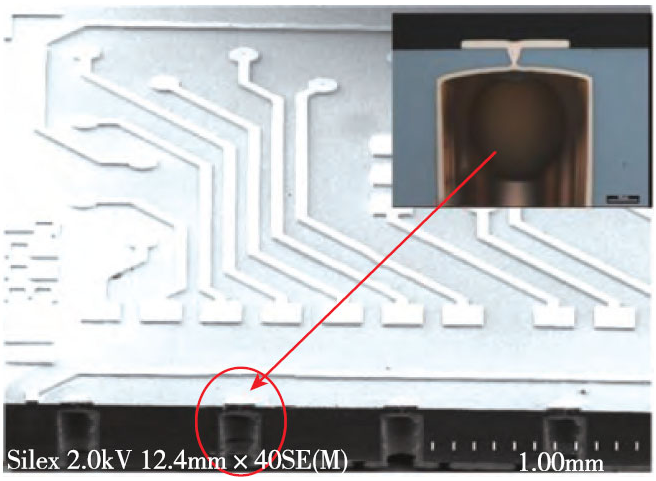

Figure 7. Metal interconnect Met-Via interconnect technology

6. CONCLUSION

Although the current MEMS inertial navigation system is used in large-scale equipment such as unmanned aerial vehicles, ground robots, etc., with the development of micro-intelligent equipment, micro-unmanned aerial vehicles, chip satellites and other high-precision inertial navigation needs are becoming increasingly strong. High-precision MEMS inertial devices are limited by the traditional packaging process and cannot be further reduced in size. The use of advanced packaging means such as three-dimensional heterogeneous heterostructure and TSV silicon adapter plate can significantly reduce the size of the MEMS inertial guidance, and promote its application in miniature intelligent equipment.

MEMS vertical interconnect technology facilitates the three-dimensional integration of MEMS chips, signal processing/decoder circuits, control chips, power supply chips, etc., by providing a vertical penetration of the adapter plate, allowing integrated components to be integrated by the functional chips fabricated with different processes on the TSV adapter plate substrate, which effectively reduces the volume/quality of the MEMS three-dimensional integration module and improves the integration degree, and can effectively reduce the volume of the The volume, mass, and thermal stress level of the inertial MEMS 3D integrated module is an important direction for the future development of inertial MEMS 3D integrated TSV interconnect technology.

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